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Docket No.: 042390.P6725

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of:

Altug Koker, et al.

Application No.: 09/372,296

Filed: August 11, 1999

For: REDUCING MEMORY ACCESS
LATENCIES FROM A BUS USING
PRE-FETCHING AND CACHING

Examiner: Jasmine Song Technology Center 2100

Art Group: 2187

AMENDMENT AND RESPONSE TO THE OFFICE ACTION

Box Non-Fee Amendment
Assistant Commissioner for Patents
Washington, DC 20231-9998

Sir:

In response to the outstanding Office Action mailed April 29, 2002, please amend the above-identified Application as follows:

IN THE SPECIFICATION

1. Please replace the paragraph beginning on page 2, line 2, with the following rewritten paragraph:

~ The present invention is a method and apparatus to reduce latency in accessing a memory from a bus. The apparatus comprises a pre-fetcher and a queue controller. The pre-fetcher pre-fetches a plurality of data from the memory to a data queue in response to a request. The queue controller is coupled to the data queue and the pre-fetcher to deliver the pre-fetched data from the data queue to the bus in a pipeline chain independently of the memory.--